Topology and Modulation for a New Multilevel Diode-Clamped Matrix Converter

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***Abstract*—To expand the matrix converter application in high power area, a new three-level diode-clamped matrix converter topology as well as a related multicarrier-based modulation scheme is proposed. The topology inherits the features from the conventional multilevel inverter and the indirect matrix converter, which is composed of a cascaded-rectifier and a three-level diode-clamped inverter. The proposed topology can overcome the voltage rating limits of the power semiconductors for high-voltage applications to some extent. Meanwhile, except the general advantages, such as bidirectional power flow, sinusoidal input and output currents, simple switch commutation, and a compact structure, it also avoids the voltage balance issue that exists in most conventional multilevel inverters. Finally, the functionality and effectiveness of the proposed topology and modulation scheme are verified by simulation and experimental results.**

***Index Terms*—Multicarrier modulation, three-level diode-clamped matrix converter (MC), voltage balance.**

I. Introduction

THE matrix converter (MC) has attracted considerable attention in recent years due to these superior features, such as bidirectional power flow, controllable input power factor, sinusoidal input and output currents, and a compact structure [1]–[5]. Due to the efforts of many researchers, it has found many applications such as adjustable-speed drives, power supply, wind energy conversion system, flexible ac transmission systems, and so on [6]–[9]. However, taking into account the limited voltage ratings of the existing power semiconductors in the market, the conventional MC is not suitable for high-voltage applications.

Usually, the multilevel concept is viewed as a good solution to high-voltage and high-power conversion. A multilevel converter can produce different output voltage levels enabling the generation of a stepped waveform with less harmonic distortion, which leads to lower *dv*/*dt* stresses, smaller common-mode voltage, and reduced voltage stress on power switches [10]. To expand the high-voltage application fields of the MC, the multilevel converter could be incorporated with the MC. Currently, a number of multilevel MC topologies have been proposed, which mainly include the multimodular MCs [11]–[14], diode-clamped MCs [15], [16], and capacitor-clamped (flying capacitor) MCs [17]–[19].

The multimodular MC inherits the topological structure of the cascaded H-bridge (CHB) converter, which uses a three-phase input/single-phase output MC as the basic unit called the module [12]. Unlike a fixed dc-link capacitor for each module in the CHB converter, each module output voltage of the multimodular MC is directly synthesized from the three phase input voltages. Certain number of modules connected in series can establish the required output voltage, but some bulky and expensive transformers would be required. Until now, the multimodular MC is the only multilevel MC product that has been commercialized. Besides, the multilevel flying capacitor MC needs excessive number of capacitors, which contradicts the original advantage of MC. And the capacitor voltage should be balanced precisely by using complicated control methods. Thus, the related contents are rarely raised as a theme for investigation by researchers.

As for the multilevel diode-clamped MC, it is built on the basis of the indirect MC generally. For instance, the three-level diode-clamped MC consists of a bidirectional current source rectifier (CSR) and a three-level diode-clamped inverter instead of the traditional two-level one. In [16], an enhanced three-level sparse topology is proposed with four active switches being saved, which can improve the output performance in terms of reduced harmonic contents. The multilevel diode-clamped MC, as well as its variants, has the ability to generate multilevel output voltages, but the input current quality may degrade to some extent. Moreover, these diode-clamped MCs still cannot overcome the voltage rating limits of power semiconductors, and it is improper to utilize them in high-voltage and high-power fields.

In this paper, a new multilevel diode-clamped MC topology is proposed, which consists of a cascaded-rectifier and a three-level diode-clamped inverter. Due to the enhanced structure, this topology can overcome the voltage rating limits of the existing power semiconductors, and has the potential to be applied in high-power areas. Moreover, it possesses the advantages of four-quadrant operation, sinusoidal input and output currents, easy commutation of switches due to the modulation strategy, and no using large energy storage elements. Compared to the traditional three-level diode-clamped inverter, it does not need to control the capacitor voltage for balance, and the neutral-point voltage is self-balanced. In addition to the topology, the related modulation scheme will be introduced in detail later, and the sinusoidal input currents are guaranteed through calculations.

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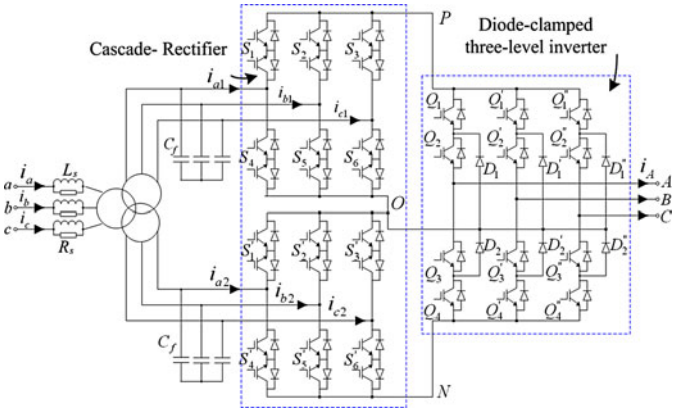

Fig. 1. Topology of the three-level diode-clamped MC.

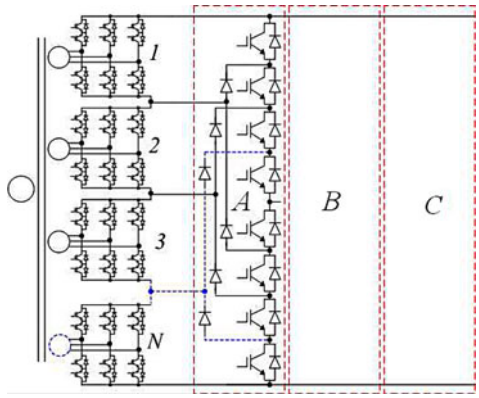

Fig. 2. Topology of the general multilevel diode-clamped MC.

The remainder of this paper is organized as follows: Section II introduces the topology of the proposed multilevel MC, as well as its extension. In Section III, the related modulation scheme is presented, followed by the input current analysis and calculations accordingly. In Section IV, the simulation and experimental results are presented, and finally, the main points of this paper are summarized in Section V.

II. Topology

The proposed three-level diode-clamped MC topology is shown in Fig. 1, which mainly consists of a second-order (*LC*) input filter, a three-phase three-winding isolated transformer, a cascaded-rectifier, and a three-level diode-clamped inverter.

In this topology, the input filter is used to prevent the harmonic currents from polluting the grid. Note that the damping resistor R_s is located in parallel with the filtering inductor L_s. And the transformer is utilized to reach the required secondary output voltage level. To alleviate the undesirable influence of the transformer leakage inductance on the power switching devices, the filtering capacitor C_f is connected to the secondary side and close to the cascaded-rectifier as much as possible. However, it is worth noting that the capacitor installed on the secondary side should be referred to the primary side, when designing the input *LC* filter.

The cascaded-rectifier is formed by two identical three-phase bidirectional CSR modules connected in series. The CSR module is composed of six bidirectional switch units (S_1–S_6 or S'_1–S'_6), and each of them is realized by two insulated-gate bipolar transistors (IGBTs) with antiparallel diode pairs connected to the common emitter. As seen in Fig. 1, the cascaded-rectifier is fed by the secondary windings of the transformer at the input side, while it provides three output terminals, i.e., P, O, and N at the output side, which are connected to the positive electrode, neutral point, and negative electrode of the dc link of the three-level diode-clamped inverter, respectively. At last, the three-level inverter undertakes the task of generating multilevel output voltage waveforms. Due to the special prestage structure, it is not necessary to place electrolytic capacitors between the dc link of the inverter. Thus, the dc-link voltage is time varying, with the input line-to-line voltages. Followed by the three-level inverter, the load could be a three-phase *RL* or a three-phase ac machine.

In fact, a general multilevel diode-clamped MC can be extended easily on the basis of the topology shown in Fig. 1. If N–1 bidirectional CSR modules are cascaded to construct a cascaded-rectifier that can provide N output terminals, the cascaded-rectifier would be connected to an N-level diode-clamped inverter. Then, the N-level diode-clamped MC will be formed, as shown in Fig. 2.

III. Modulation Scheme

Similar to the indirect MC, the modulation scheme for the proposed multilevel topology could also be divided into two sections, which is easier to understand. For the cascaded-rectifier, the space vector pulsewidth modulation (SVPWM) is adopted, while for the three-level diode-clamped inverter, a multicarrier-based modulation method is proposed for the reduction of computational burden.

A. SVPWM for the Rectifier

The purpose of the rectifier is to generate the desired input currents, controllable input power factor, and a positive dc-link voltage, which will be realized with SVPWM by modulating two line-to-line input voltages. The current space vector diagram for the rectifier modulation is shown in Fig. 3. As seen, six active vectors I_1–I_6 and three zero vectors I_7–I_9 can be used to synthesize the desired input current vector $\vec{i}$, where each vector corresponds to a switching state of the rectifier.

Based on the current space vector synthesis principle, the duty ratios of the adjacent active vectors can be expressed as follows:

$$\begin{cases} d_\alpha = \sin\left(\pi/6 - [\theta - (n-1)\,\pi/3]\right) \\ d_\beta = \sin\left(\pi/6 + [\theta - (n-1)\,\pi/3]\right) \\ d_0 = 1 - d_\alpha - d_\beta \end{cases} \tag{1}$$

where d_α, d_β, and d_0 are the duty ratios of the active and zero vectors, respectively. θ represents the angular position of the current vector, and $n\,(n = 1, 2, \ldots, 6)$ denotes the current vector sector.

Generally, only the active vectors (no zero vectors) are used here to reduce the commutation times, which also can maximize

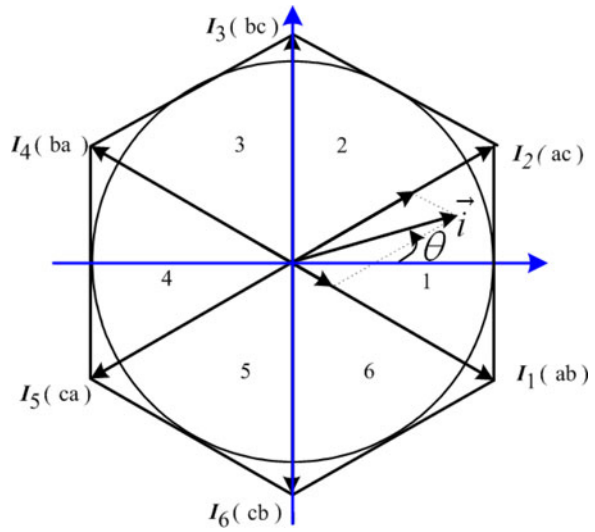

Fig. 3. Space vector diagram for the rectifier modulation.

the voltage utilization and make the following carrier-based modulation easy to implement. Therefore, the corresponding duty ratios are normalized as follows:

$$\begin{cases} d_\alpha = \dfrac{d_1}{(d_1+d_2)} = k(\theta)\sin(\pi/6 - [\theta-(n-1)\pi/3]) \\ d_\beta = \dfrac{d_1}{(d_1+d_2)} = k(\theta)\sin(\pi/6 + [\theta-(n-1)\pi/3]) \end{cases} \tag{2}$$

where

$$k(\theta) = \frac{1}{\cos[\theta-(n-1)\pi/3]}.$$

The completely identical modulation scheme is used in each matrix rectifier module of the cascade-rectifier, and then, a neutral point for the three-level diode-clamped inverter is formed naturally. The switching pattern of the cascaded-rectifier is shown Fig. 4(a), if the desired input current vector lying within sector 1 is considered.

If the proposed topology works at unity input displacement factor, the average dc-link voltage during each switching period can be calculated as

$$u_{pn} = u_{\rm dc} = 3k(\theta)U_{im} \tag{3}$$

where U_{im} is the amplitude of the input phase voltage referred to the transformer secondary side. From (3), it can be found that the dc-link voltage will show a fluctuation with six times the input voltage frequency.

As far as the N-level MC is concerned, the SVPWM mentioned previously can still be used in all N–1 CSR modules, which would yield N levels for the dc-link voltage ultimately, at any instant.

B. Multicarrier Modulation for the Inverter

As well known, both the SVPWM and multicarrier-based PWM can be viewed as the commonly used methods in multilevel inverter [10]. However, the SVPWM becomes difficult to

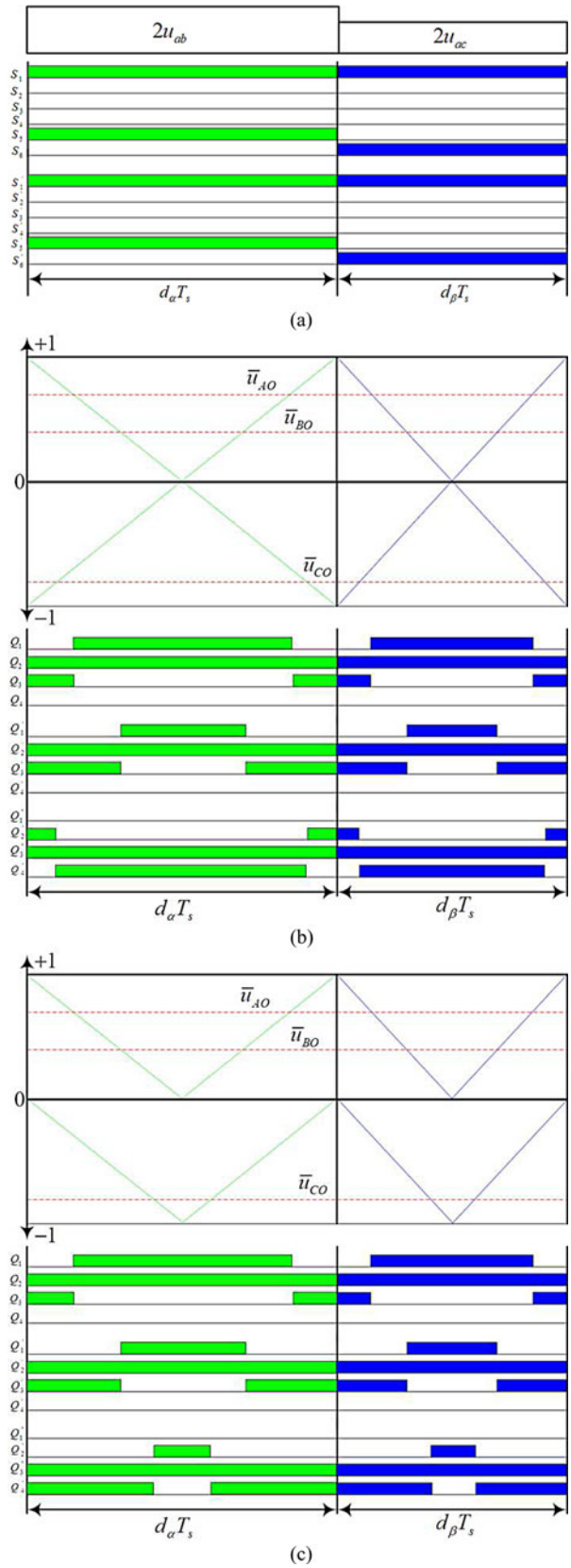

Fig. 4. Schematic diagrams and related switching patterns of the proposed modulation: (a) rectifier, (b) inverter POD, and (c) inverter PD.

implement, when the level number of the inverter gets higher. For simplicity, the carrier-based PWM idea is utilized in this section. Due to the fact that the operating principle of the MC is different from that of the conventional inverter, the classic multicarrier-based PWM cannot be applied here directly. Therefore, the derivation of multicarrier-based PWM for MC will be introduced as follows.

Assume that the output phase voltages are

$$\begin{cases} u_A = U_{om}\cos(\omega_o t) \\ u_B = U_{om}\cos(\omega_o t - 2\pi/3) \\ u_C = U_{om}\cos(\omega_o t + 2\pi/3) \end{cases} \tag{4}$$

where u_A, u_B, and u_C are the desired output phase voltage, and U_{om} and ω_o are the amplitude and angular frequency of the output voltages, respectively.

According to Fig. 1, it yields

$$\begin{cases} u_{AO} = u_A + u_{NO} \\ u_{BO} = u_B + u_{NO} \\ u_{CO} = u_C + u_{NO} \end{cases} \tag{5}$$

where u_{AO}, u_{BO}, and u_{CO} are the modulated signals, and u_{NO} denotes the zero-sequence signal. Usually, to maximize the utilization of the dc-link voltage, the zero-sequence signal u_{NO} is chosen by

$$u_{NO} = -\frac{\min(u_A, u_B, u_C) + \max(u_A, u_B, u_C)}{2}. \tag{6}$$

For the convenience of analysis and implementation, the modulated signals u_{AO}, u_{BO}, and u_{CO} are normalized as

$$\bar{u}_{iO} = 2\frac{u_{iO}}{u_{\rm dc}},\ i \in \{A, B, C\} \tag{7}$$

with the constraint

$$-1 \le \bar{u}_{iO} \le 1 \tag{8}$$

where the variables overlined, i.e., $\bar{u}_{iO}$ denote the normalized values.

In this scheme, the modulation period T_s is divided into two time-varying subperiods $d_\alpha T_s$ and $d_\beta T_s$, due to the fact that the dc-link voltage is formed by two input line-to-line voltages obtained from the rectifier. Thus, the conventional carrier-based modulation process occurs twice in one switching period, and the carrier frequency will vary with time. Furthermore, there are two carriers exist at any instant for the three-level converter, instead of the common carrier for three modulated signals in the conventional two-level inverter, which we can call the multicarrier-based PWM. In general, the phase disposition (PD) and phase opposition disposition (POD) methods are commonly used [20]. In such methods, the PD method can lead to the lower line voltage harmonic distortion, while the POD method enable to provide zero current commutation for the rectifier, which can reduce the switching loss and improve the reliability of MC.

Under the condition $\bar{u}_{AO} > \bar{u}_{BO} > \bar{u}_{CO}$, Fig. 4(b) and (c) demonstrates the schematic diagrams and related switching patterns of the POD and PD methods, respectively. As seen in Fig. 4(b), the inverter switches $(Q_1, Q_4, Q_1', Q_4', Q_1''$, and $Q_4'')$ are always OFF, when the rectifier switches need to be commutated. But in Fig. 4(c), Q_3'' and Q_4'' are ON, and the rectifier switches cannot reach zero current commutation. Moreover, if one of the modulated signals changes its sign in the next modulation period, there would be multiple switches in both the rectifier and inverter that are required to commutate simultaneously, which is complicated and not easy to deal with. Therefore, considering the commutation issues, the POD method is adopted here.

For the N-level inverter, with the N levels of dc-link voltage obtained from the rectifier, the multicarrier-based method can still be applied; in this case, N–1 carriers should be used.

C. Input Current Derivations

For the proposed multilevel MC, the goal of sinusoidal input and output currents should be guaranteed first, under the balanced three-phase loads. Usually, by properly synthesizing the balanced and sinusoidal output voltages, it is not difficult to obtain the desired sinusoidal output currents. However, under the proposed modulation method, whether the sinusoidal input currents could be acquired should be considered carefully. Thus, this section gives a detailed analysis for it with the derivation of its analytical formula.

Assume that the three-phase output currents $(i_A, i_B$, and $i_C)$ are sinusoidal and balanced, and the transformer ratio used in this topology is N_p/N_s. Neglecting the currents through the filter capacitors and magnetizing inductance in the isolated transformer, according to Fig. 1, the input currents could be expressed as follows:

$$\begin{cases} i_a = \dfrac{N_s}{N_p}(i_{a1} + i_{a2}) \\ i_b = \dfrac{N_s}{N_p}(i_{b1} + i_{b2}) \\ i_c = \dfrac{N_s}{N_p}(i_{c1} + i_{c2}). \end{cases} \tag{9}$$

For simplicity, only a-phase input current is considered first. In (9), i_{a1} and i_{a2} are the a-phase current of the two CSR modules. Without loss of generality, if the desired input current vector lies in sector 1, i_{a1} and i_{a2} in the average sense can be given as

$$\begin{cases} i_{a1} = (d_\alpha + d_\beta)(d_{Ap} i_A + d_{Bp} i_B + d_{Cp} i_C) \\ i_{a2} = -(d_\alpha + d_\beta)(d_{An} i_A + d_{Bn} i_B + d_{Cn} i_C) \end{cases} \tag{10}$$

where d_{ip} and d_{in} $(i \in \{A, B, C\})$ represent the duty ratios of the switching states S_{ip} and S_{in} in the inverter, respectively.

Take the A-phase leg of the inverter shown in Fig. 1, for example, S_{Ap} denotes the switching state: Q_1 and Q_2 are ON, Q_3 and Q_4 are OFF; while S_{An} denotes the opposite state: Q_1 and Q_2 are OFF, Q_3 and Q_4 are ON. According to Fig. 4(b), d_{ip} and d_{in} can be expressed as

$$d_{ip} = \begin{cases} \bar{u}_{iO}, & \text{when } \bar{u}_{iO} \ge 0 \\ 0, & \text{when } \bar{u}_{iO} < 0 \end{cases} \tag{11}$$

$$d_{in} = \begin{cases} 0, & \text{when } \bar{u}_{iO} \ge 0 \\ -\bar{u}_{iO}, & \text{when } \bar{u}_{iO} < 0. \end{cases} \tag{12}$$

TABLE I
PARAMETERS USED IN THE SIMULATIONS

Parameters	Value
Input voltage (U_i)	220V
Filter inductor (L_s)	1.0mH
Filter capacitor (C_f)	30μF
Damping resistor (R_s)	50Ω
Resistor of load (R)	12.5Ω
Inductor of load (L_o)	4.5mH
Switching frequency (f_s)	5kHz
Transformer ratio (N_p/N_s)	11/3

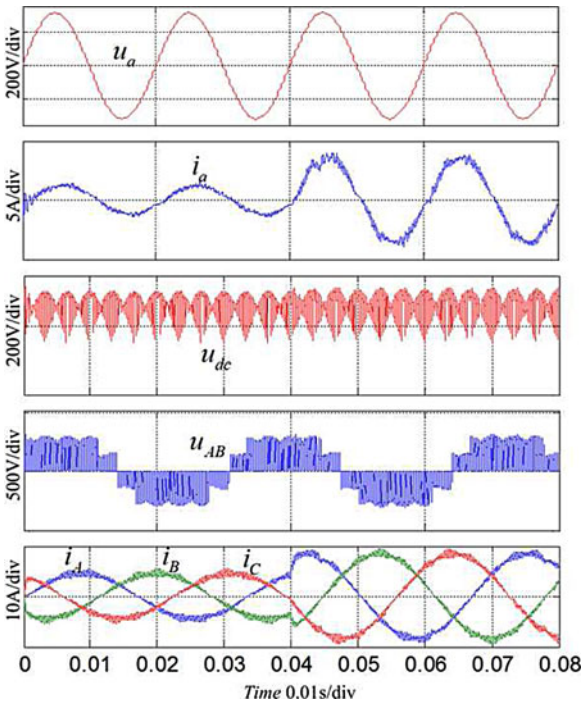

Fig. 5. Simulation results with the desired output voltage changing from 60 V/30 Hz to 110 V/30 Hz.

In that case, if substituting (10) into (9), it leads to

$$i_a = \frac{N_s}{N_p}[(d_{Ap} - d_{An})\, i_A + (d_{Bp} - d_{Bn})\, i_B + (d_{Cp} - d_{Cn})\, i_C]. \tag{13}$$

Then, after some manipulations with (3), (7), (11), and (12), i_a can be written as

$$i_a = \frac{2N_s P_o}{3N_p U_{im}} \cos(\theta) = I_{im} \cos(\theta) \tag{14}$$

where I_{im} denotes the input current amplitude, $P_o = u_A i_A + u_B i_B + u_C i_C$, and it represents the output active power.

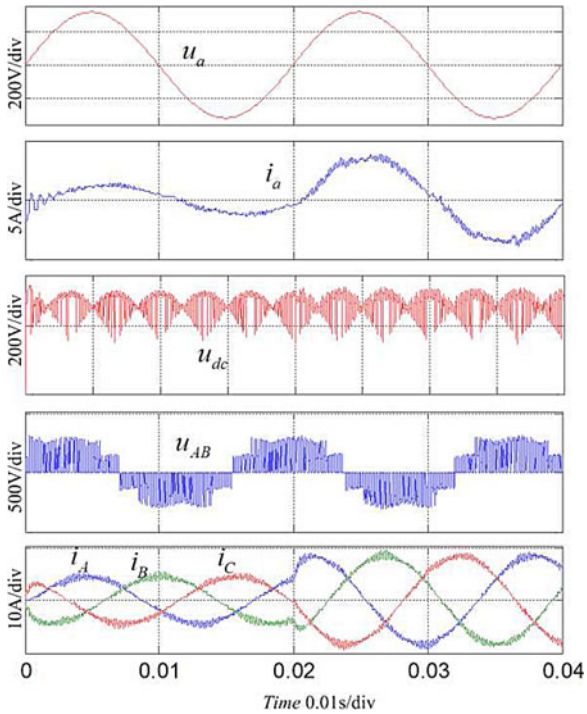

Fig. 6. Simulation results with the desired output voltage changing from 60 V/60 Hz to 110 V/60 Hz.

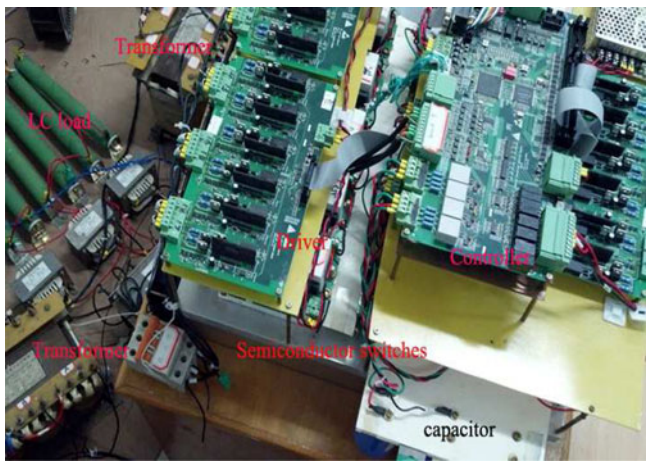

Fig. 7. Experimental setup for the three-level diode-clamped MC.

Similarly, the b- and c-phase input currents (i_b and i_c) could also be obtained as follows:

$$i_b = -\frac{N_s}{N_p} d_\alpha \left(\bar{u}_{Ao} i_A + \bar{u}_{Bo} i_B + \bar{u}_{Co} i_C\right) = I_{im} \cos(\theta - 2\pi/3) \tag{15}$$

$$i_c = -\frac{N_s}{N_p} d_\beta \left(\bar{u}_{Ao} i_A + \bar{u}_{Bo} i_B + \bar{u}_{Co} i_C\right) = I_{im} \cos(\theta + 2\pi/3). \tag{16}$$

If the desired input current vector lies in other sectors, the similar conclusions can also be obtained. Therefore, from (14) to (16), it proves in theory that, under the given balanced input

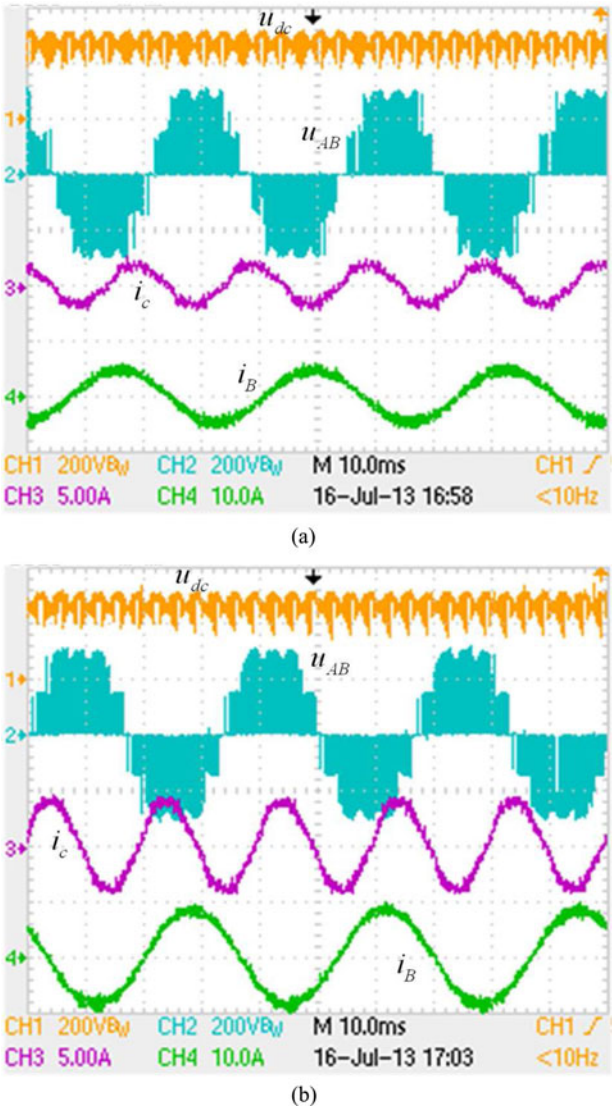

Fig. 8. Experimental waveforms with different desired output voltages: (a) 60 V/30 Hz and (b) 110 V/30 Hz.

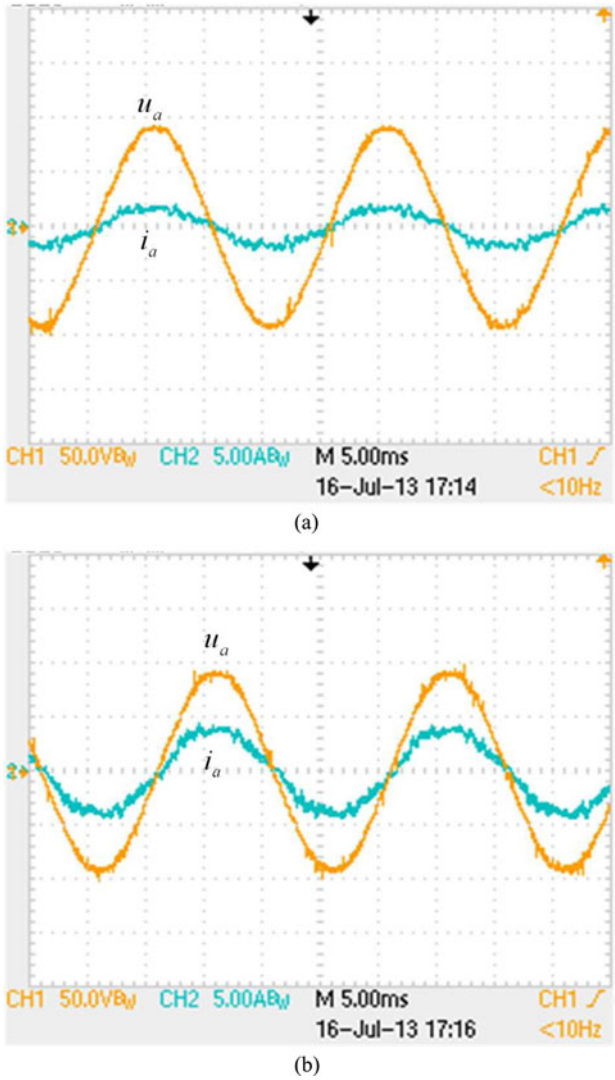

Fig. 9. Input voltage and current waveforms with different desired output voltages: (a) 60 V/30 Hz and (b) 110 V/30 Hz.

voltages, the average input currents of the proposed multilevel MC are sinusoidal and balanced, with the proposed modulation scheme.

IV. Simulation and Experimental Results

A. Simulation Results

To verify the functionality and effectiveness of the proposed three-level diode-clamped MC topology (as shown in Fig. 1) and the modulation scheme, some numerical simulations are carried out by using MATLAB/Simulink. All the semiconductor switches, inductors, capacitors, and transformers used in the simulations are chosen from the power system block set in the Simulink, and we do not take into account dead-time but the device voltage drops. The related parameters are listed in Table I, and a three-phase balanced *RL* load is utilized.

First, the desired output voltage is arranged as follows: before 0.04 s, it is set to 60 V/30 Hz, and after 0.04 s, it is set to 110 V/30 Hz. Fig. 5 shows the simulation waveforms (from up to down) of the a-phase input voltage u_a, a-phase input current i_a, dc-link voltage $u_{\rm dc}$, output line-to-line voltage u_{AB}, and three phase load currents i_A, i_B, and i_C.

As seen, the load currents are balanced and sinusoidal, which means that the desired output voltages are obtained. The input current is almost sinusoidal, and in phase with the corresponding input phase voltage. With the increase of the desired output voltage, both the input and output currents increase suddenly at $t = 0.04$ s, and some slight variations also appear in the waveform of $u_{\rm dc}$. That is because the increased output power would yield a larger input voltage ripple for $u_{\rm dc}$. Moreover, it can be found from Fig. 5 that the output line-to-line voltage has three distinct levels: dc-link voltage, half dc-link voltage, and zero voltage.

Similarly, if the desired output voltage changes from 60 V/60 Hz to 110 V/60 Hz at $t = 0.02$ s, the corresponding simulation results are illustrated in Fig. 6.

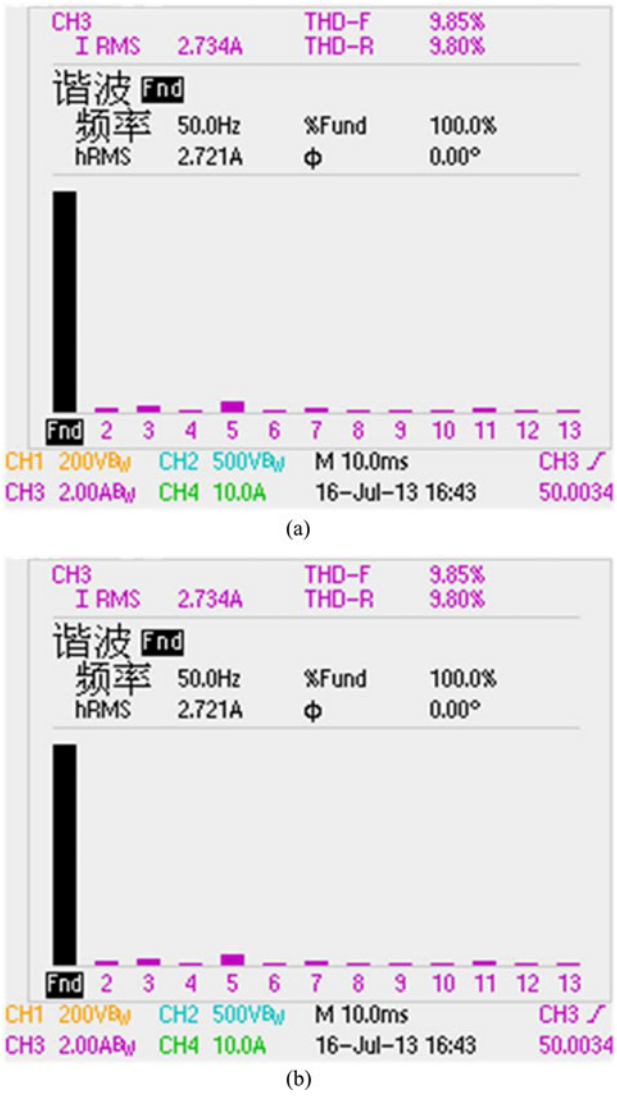

Fig. 10. Spectrum graphics of the input current with different desired output voltages: (a) 60 V/30 Hz and (b) 110 V/30 Hz.

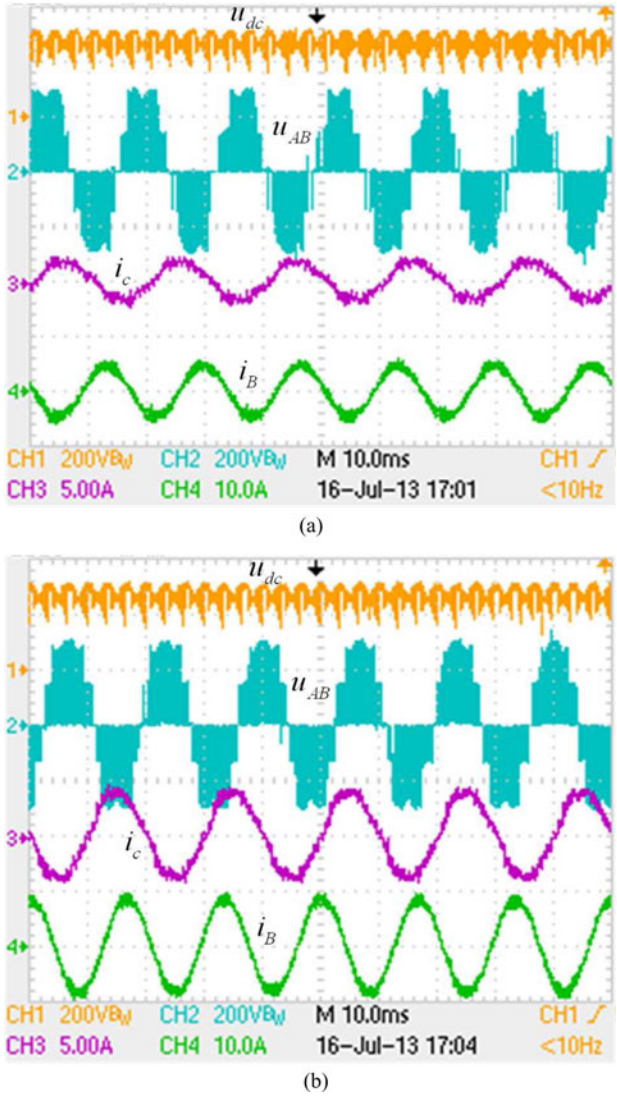

Fig. 11. Measured waveforms: (a) output voltage of 60 V/60 Hz and (b) output voltage of 110 V/60 Hz.

B. Experimental Results

To validate the proposed topology and its modulation scheme experimentally, an experimental setup for the three-level diode-clamped MC has been developed in the laboratory, as shown in Fig. 7. The IGBT module (FF300R12KT3_E) with common emitter is used as the bidirectional switch in the rectifier. The inverter consists of three pairs of IGBT modules (F3300R12ME4_B23 and F3300R12ME4_B23). The controller board is mainly composed of a floating-point DSP (TMS320F28335) and a field-programmable gate array (EP2C8J144C8N). To form isolated power supplies for the MC, two step-down transformers (220 V/60 V) are employed. The corresponding parameters are the same as those in the simulations.

Fig. 8(a) and (b) shows the experimental waveforms of the dc-link voltage $u_{\rm dc}$, output line-to-line voltage u_{AB}, input current i_c, and output current i_B, when the desired output voltage is set to 60 V/30 Hz and 110 V/30 Hz. As seen, the output line-to-line voltage is characterized by three levels, which is different from the "three-level voltage" of the conventional MC.

Fig. 9 shows the experimental waveforms of the input voltage u_a and input current i_a, under the same operating conditions as those in Fig. 8. As seen, the input current is almost in phase with the input voltage, which means that unity input power factor has been achieved. The corresponding spectrum analysis results of the input current are demonstrated in Fig. 10. As indicated by the graphics, in both cases, the fifth-order harmonic content is the largest one, but the total harmonic distortion in the case of 60 V/30 Hz is higher than that when the desired output voltage is set to 110 V/30 Hz. The distorted current is mainly caused by the dead-time, device voltage drop, distorted no-load current in the transformer, and so on.

When the frequency of desired output voltage changes from 30 to 60 Hz, the related experimental results are shown in Fig. 11. Since the load impedance variation is small, there are not significant changes for the experimental waveforms except for the

output frequency. It can be found that the experimental results agree well with the simulation results.

V. Conclusion

This paper proposed a new three-level diode-clamped MC topology for high-voltage and high-power application, which is easy to be extended to a generalized multilevel diode-clamped topology. Moreover, a multicarrier-based PWM scheme featured by varying carrier frequency is presented to reduce the realization effort. By using the scheme, zero current commutation for the rectifier can be realized, which has lower switching loss and better reliability. Some numerical simulations and experiments have been performed, and the results have verified the feasibility of the proposed topology and the modulation scheme.

Compared to the traditional diode-clamped inverter, the proposed converter belongs to the category of the diode-clamped MCs, which can offer bidirectional energy flow, and avoid bulky energy storage element and additional voltage balance control.

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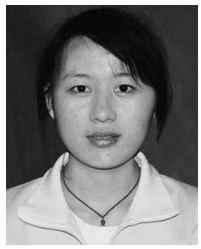

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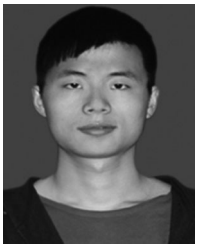

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